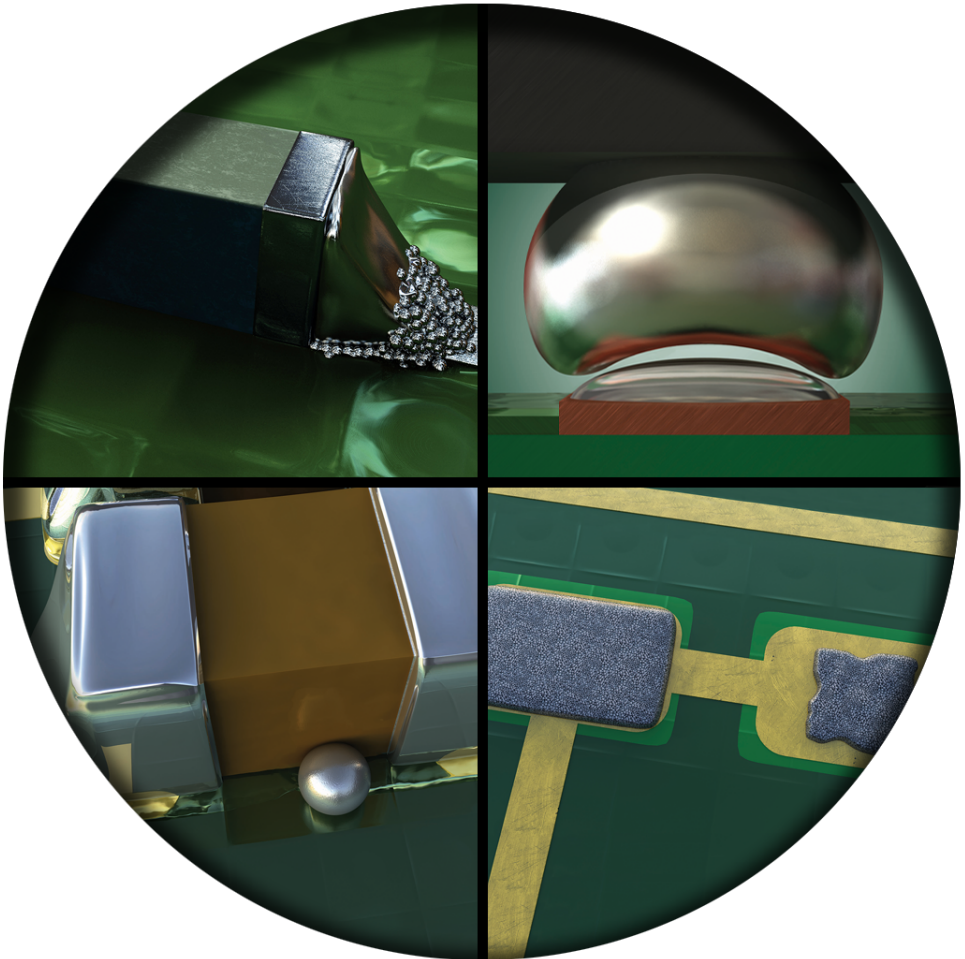


THE PRINTED CIRCUIT ASSEMBLER'S GUIDE TO...™

SOLDER DEFECTS



Christopher Nash and
Dr. Ronald C. Lasky
Indium Corporation

The Printed Circuit Assembler's Guide to...™

SOLDER DEFECTS

Christopher Nash
Dr. Ronald C. Lasky

Indium Corporation

© 2021 BR Publishing, Inc.
All rights reserved.

BR Publishing, Inc.
dba: I-Connect007
942 Windermere Dr. NW
Salem, OR 97304
U.S.A.

ISBN: 978-1-7370232-7-2



Visit I-007eBooks.com for more books in this series.

I-Connect007
GOOD FOR THE INDUSTRY

I-Connect007.com

MEET THE AUTHORS



Christopher Nash

Chris Nash is the Senior Product Manager for Indium Corporation's PCB Assembly Solder Paste. With an intimate understanding of customer needs and challenges, he works closely with the company's R&D team to deliver fully scaled, launched, marketable product solutions for the PCB assembly market. Chris also provides comprehensive technical advice

in the selection, use, and application of solder paste and flux to electronics assembly customers throughout the world. He is responsible for ensuring the product line is poised for future growth to best meet the needs of existing and potential customers.

Chris joined Indium Corporation in 2005. He has authored several process and technical guidelines and has presented at numerous industry forums and conferences. He is a member of the SMTA and participates in the occasional IPC standards development committee.

Chris has a bachelor's degree from Clarkson University. He is certified as a Six Sigma Green Belt from Dartmouth College's Thayer School of Engineering and is a certified SMT process engineer.



Dr. Ronald C. Lasky

Dr. Ronald Lasky is a senior technologist at Indium Corporation, as well as a professor of engineering at Dartmouth College. He has more than 30 years of experience in electronics and optoelectronics packaging at IBM, Universal Instruments, and Cookson Electronics.

Dr. Lasky has authored six books, and contributed to nine more, on science, electronics, and optoelectronics, and has authored numerous technical papers. Additionally, he has served as an adjunct professor at several colleges, teaching more than 20 different courses

on topics ranging from electronics packaging, materials science, physics, mechanical engineering and science, and religion.

Dr. Lasky holds numerous patent disclosures and is the developer of several SMT processing software products relating to cost estimating, line balancing, and process optimization. He is the co-creator of engineering certification exams that set standards in the electronics assembly industry worldwide. Dr. Lasky was awarded the Surface Mount Technology Association's Founder's Award in 2003.

Dr. Lasky holds four degrees, including a Ph.D. from Cornell University in materials science, and is a licensed professional engineer. He lives with his wife in Vermont.

MEET THE PEER REVIEWER

This book has been reviewed for technical accuracy by the following expert from the PCB industry.



Joseph O'Neil

Joseph O'Neil has nearly 30 years of experience in the electronic manufacturing services (EMS) sector. He serves as chairman of the IPC Education Foundation and has served on the IPC Board for over 12 years. Joe was formerly the owner and CEO of Hunter Technology, which grew from 80 to 360 employees during his tenure. He obtained his Bachelor of Business Administration degree with emphasis in finance and management from Loyola Marymount University.

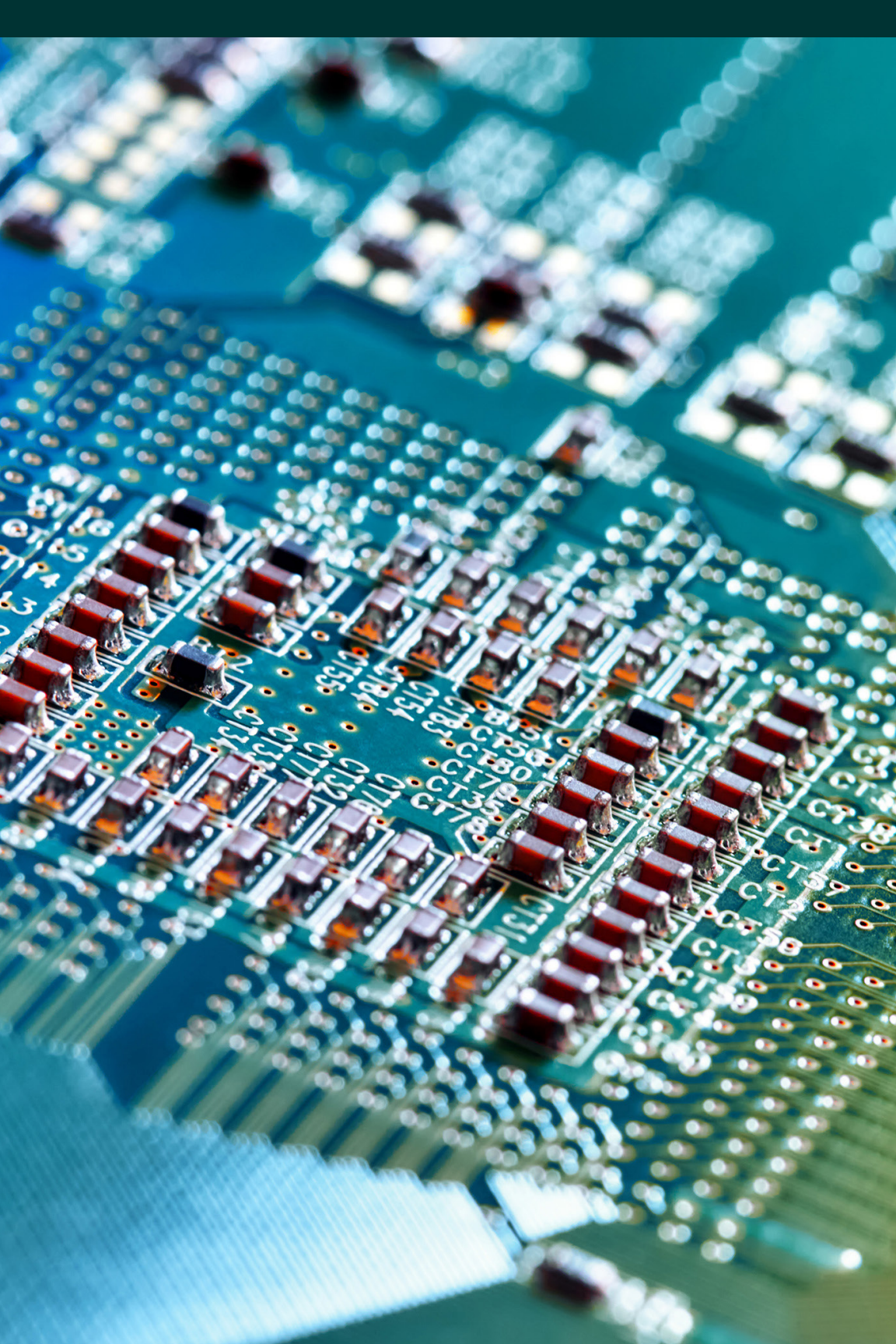
Joe currently advises clients through his firm, OAA Ventures, which he founded in 2015 following the acquisition of Hunter Technology by Sparton Corporation. OAA Ventures provides consulting and advisory services to electronic manufacturing service providers, printed circuit board fabricators, and technology start-ups.

Joe currently advises clients through his firm, OAA Ventures, which he founded in 2015 following the acquisition of Hunter Technology by Sparton Corporation. OAA Ventures provides consulting and advisory services to electronic manufacturing service providers, printed circuit board fabricators, and technology start-ups.



Contents

1	Introduction
	Chapter 1:
3	Minimizing Voiding in SMT Assembly
	Chapter 2:
9	Graping
	Chapter 3:
15	The Head-in-Pillow and Non-Wet Open Defects
	Chapter 4:
21	Tombstoning of Passive Components
	Chapter 5:
27	Solder Paste Insufficients
	Chapter 6:
33	Solder Balling and Beading
40	Conclusion
41	References
43	About Indium Corporation



Introduction

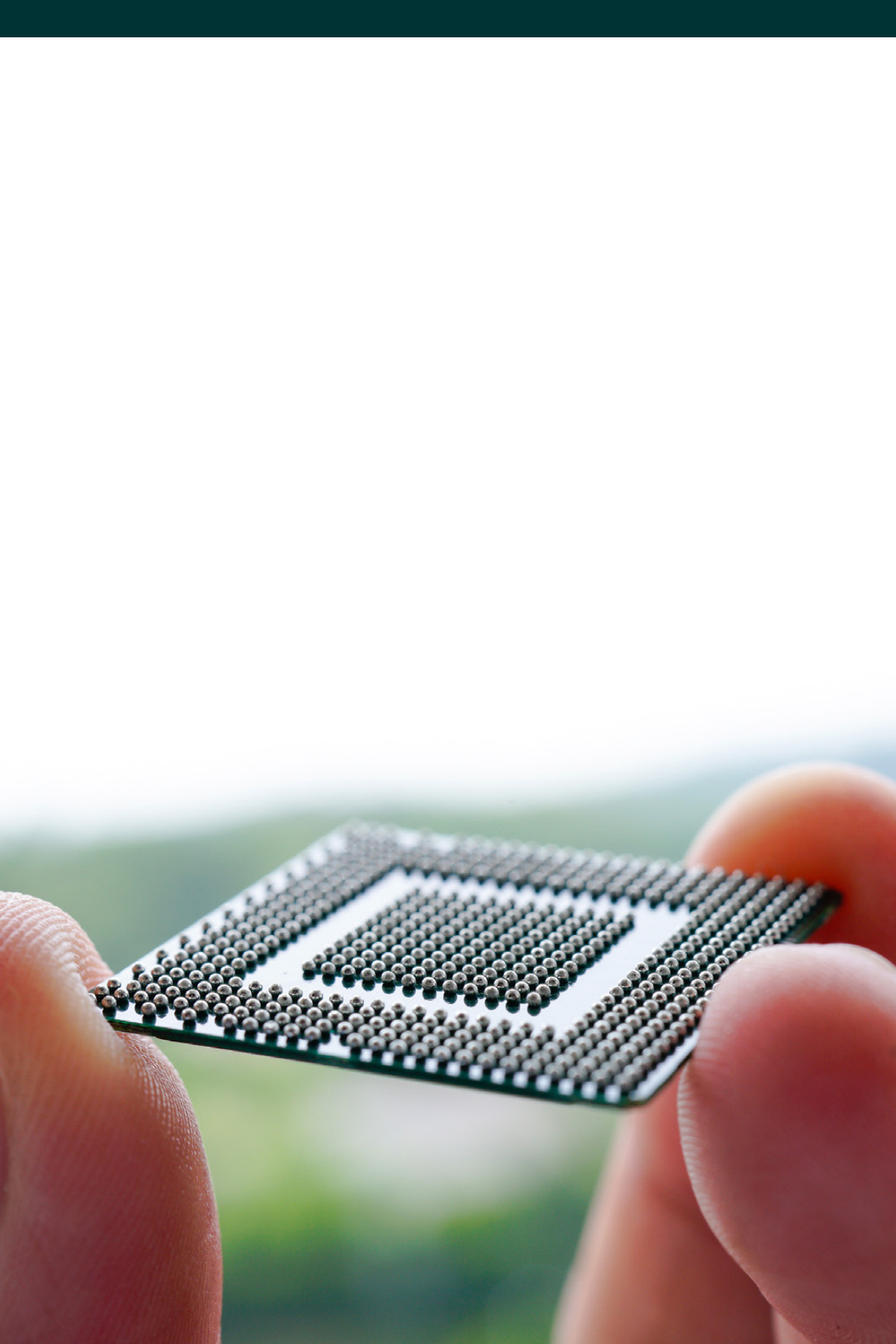
In 2006, much of the world switched from tin-lead to lead-free solder. The European Union's Restriction of Hazardous Substances (RoHS) directive, which essentially eliminated lead from electrical solder, drove this global move. This change has challenged circuit board assemblers since Pb-free solders melt at temperatures nearly 40°C hotter than lead-containing solders, and they do not flow or wet as well as SnPb solders.

At the same time, the density of electronics has unabatedly increased. This density increase has resulted in exponentially more powerful electronics—the fastest supercomputer of 1996 is outperformed by today's iPhone 11 Pro—creating another challenge for assemblers. Whereas the 0402 passive was the leading edge in miniaturization in the SnPb era, the 0201, 01005, and smaller passives have emerged for Pb-free soldering. The combined challenges of Pb-free soldering and ever-increasing miniaturization have resulted in new or exacerbated defects in electronics assembly. This book was developed to address this problem, and will address the following defect topics:

1. **Voiding in SMT Assembly**
2. **Graping**
3. **Head-in-Pillow and Non-Wet Open Defects**
4. **Tombstoning of Passive Components**
5. **Solder Paste Insufficients**
6. **Solder Balling and Beading**

It is also important to recognize that effective electronics assembly is an optimization process—often, minimizing one defect will exacerbate another. So, in addition to the information presented here, when confronted with a process defect or challenge, it is helpful to refer to experts from your materials or equipment suppliers. IPC and SMTA standards should provide further guidance as well, along with the many excellent courses presented by these industry organizations.

It is our hope that this book will be beneficial to PCB assemblers in improving their assembly processes. We would also be delighted to address any issues not discussed in this book. Please contact us with your questions at: askus@indium.com or visit us online at indium.com.



Minimizing Voiding at SMT Assembly

Voiding has been an issue in surface mount technology (SMT) assembly for decades. In the past, voiding has been generally connected to ball grid array (BGA) balls and, to a lesser extent, solder joints. The advent of Pb-free soldering in the mid-2000s has increased the occurrence of these types of voids. These voids can cause reliability issues related to thermal cycling crack propagation.

More recently, voiding has become more prevalent in bottom termination components (BTCs). Voiding can occur during soldering of the BTC thermal pads to the printed wiring board (PWB). These voids can result in poor heat transfer from the BTC, and compromise thermal reliability for the BTC's integrated circuit.

This chapter will address both of these voiding concerns.

Voiding in BGA Solder Joints

Early studies indicated that Pb-free assembly created more voids in solder joints than SnPb assembly. This fact was attributed to Pb-free solders driving off more flux volatiles at the higher reflow temperatures and to slower wetting speeds. This defect was especially common in BGA and chip-scale package (CSP) solder balls. To minimize this type of voiding, a hot soak profile was shown to be successful (Figure 1.1). This success is attributed to the larger concentration of flux volatiles being driven off before the solder balls melt.

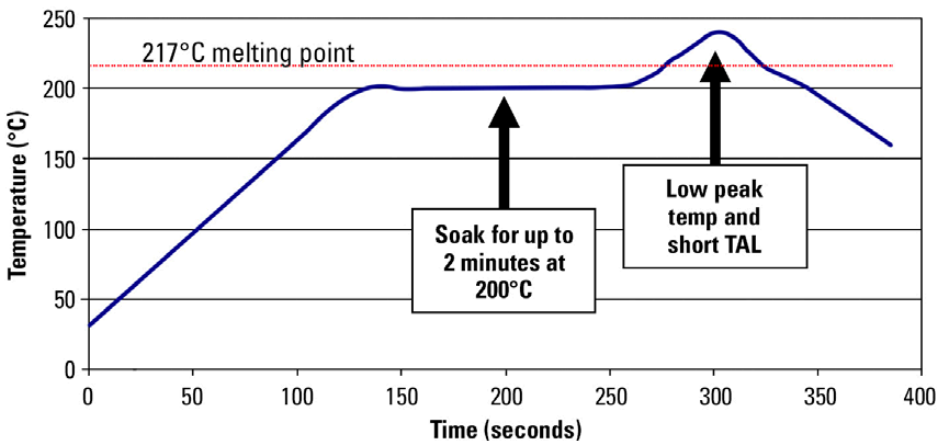


Figure 1.1: A hot soak profile can minimize voiding in BGA and CSP solder balls.

Electronics assembly is inherently an optimization process. While the profile in Figure 1.1 may minimize voiding, it may also result in other failure mechanisms. However, if a process is producing voiding in BGA solder joints, the voiding will be minimized if a reflow profile similar to that of Figure 1.1 is used.

Voiding in Bottom Termination Components

The bottom termination component is one of the most important elements in electronics today. The combination of small size, excellent electrical performance, and the ability to transfer heat away from the integrated circuit (IC) has resulted in BTCs becoming one of the most common packages with the highest growth rate.

Since one of the main strengths of quad-flat no-leads (QFNs) is dissipating heat, any solder voiding connecting the QFN's thermal pad to the PWB will degrade the intended performance of the QFN component. This degraded thermal performance may result in operability and reliability issues.

Discussions with electronics assemblers have led to the conclusion that voiding in BTCs, and more specifically QFNs, is arguably the most critical issue in electronics assembly today.

The industry standard for an acceptable voiding level has not yet been established. However, there is general agreement that an average void area should consist of less than 50%, with no single void above 40%. For thermal pads, a void area of less than 25% is often preferred. Some automotive applications

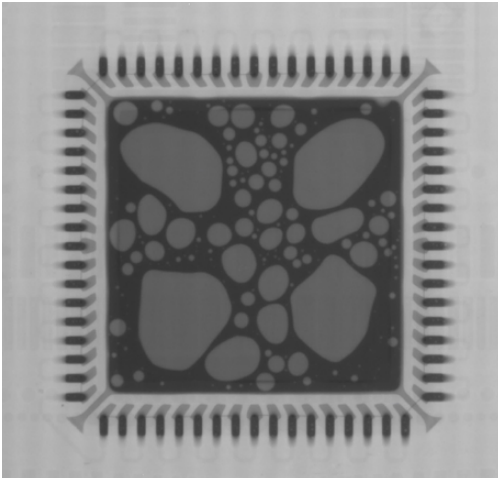


Figure 1.2: X-ray images of voiding. These “lake voids” with a >40% area of voiding would likely cause reliability and performance problems for most QFNs.

demand an average void area of less than 10%. While all assemblers desire a minimum amount of voiding, especially to avoid the situation shown in Figure 1.2, current processes and available materials may limit this goal.

Significantly reducing voiding is not necessarily a quick fix. In addition to controlling the PWB and components, you also need to optimize the solder paste and process conditions, stencil printer, component placement equipment, and reflow oven.

Determining the parameters to reduce voiding is not trivial. Consider the Large Ground Plane Voiding Ishikawa (cause and effect) diagram shown in Figure 1.3.

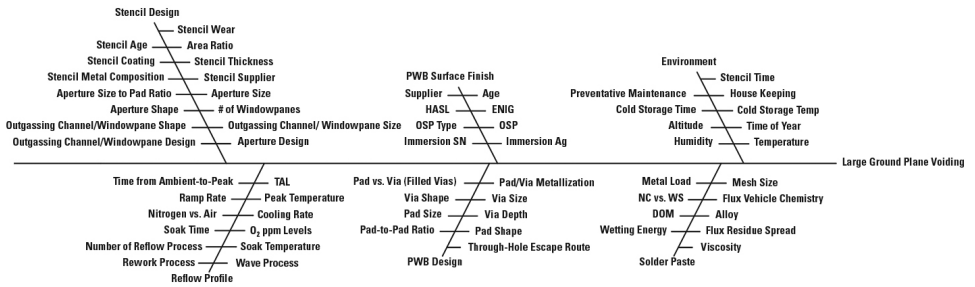


Figure 1.3: Many parameters affect voiding, as seen in the above Ishikawa (cause and effect) diagram.

Stencil Design

It has been shown that a thicker stencil exhibits less void area because the higher standoff (0.005" vs. 0.004") allows for easier outgassing/venting of the solder paste flux volatiles.

The aperture design can also have a major effect on voiding. It is often recommended that a windowpane aperture design be employed in BTCs to allow for outgassing channels. However, the size of the windowpane is a delicate balance. Too large of a pane may create a void if the solder paste doesn't wet out to fill in the outgassing channel, especially in Pb-free assemblies, as the solder will not spread as much as SnPb alloys. Conversely, a small outgassing channel may close too quickly as the solder spreads, and there may not be enough time for the flux volatiles to escape. BGA and LGA voiding are also affected by the aperture design, and certain aperture shapes can be used to reduce voiding levels.

Solder Paste Particle Size

Experiments have been performed varying the solder paste particle size. Results indicate a slight reduction in void area with small solder paste particle sizes from Types 4 to 4.5 to 5. However, there is a significant increase in voiding area with Type 3 paste.

Solder Pastes

We have evaluated the effect of different solder paste flux vehicles on voiding. Some pastes produced approximately 5% voids, while others produced as much as 45%. These results were not only surprising, but also very encouraging.

These types of differences are seen in Figure 1.4, which shows the void percent area as a function of solder pastes. There is a significant difference between pastes, some giving as low as 5% voids, and others 45%.

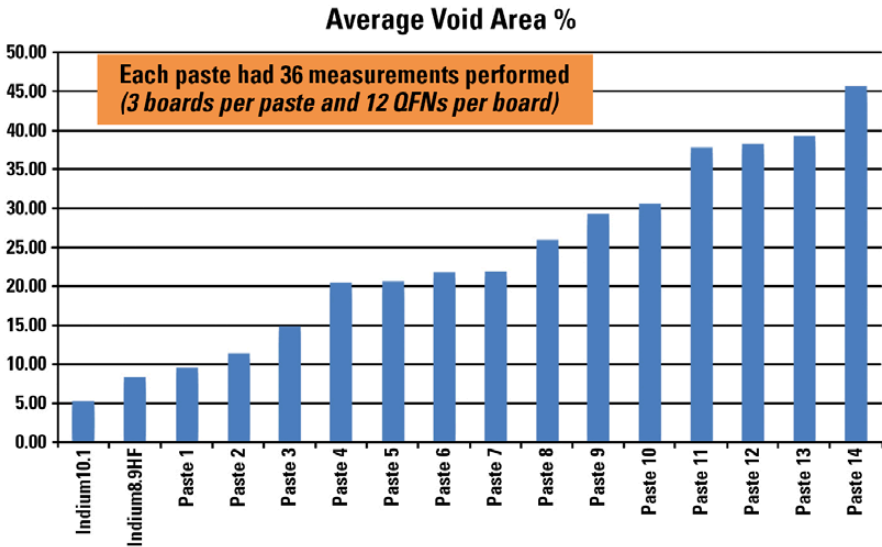


Figure 1.4: While the generation of voids is a complicated process with many variables, selecting singularly the solder paste with a standard assembly process can assure voiding area levels of less than 10%.

Board Design

Pad and mask design surface and finish can also be optimized to help reduce voiding. Studies have shown that adding solder mask and splitting the large ground pad into multiple smaller pads can reduce voiding, as this provides permanent outgassing channels for the flux volatiles to escape. Through-hole vias in the ground pad are another way to add permanent outgassing channels. However, it is possible for the solder to wet down into the vias, potentially causing lower standoff height of even starvation voids, which could make voiding worse.

There are several common surface finish options and not all are created equal. Some will oxidize more readily than others which will make the challenge of lowering voiding more challenging. Even the type of oxidation can play a role. For instance, SnO_2 will be more difficult to clean. Some surface finishes will allow for better wetting, which could improve voiding performance. However, competitive solder pastes should work well with all surface finishes to reduce voiding. And of course, cleanliness and age of the board will also yield varying results.

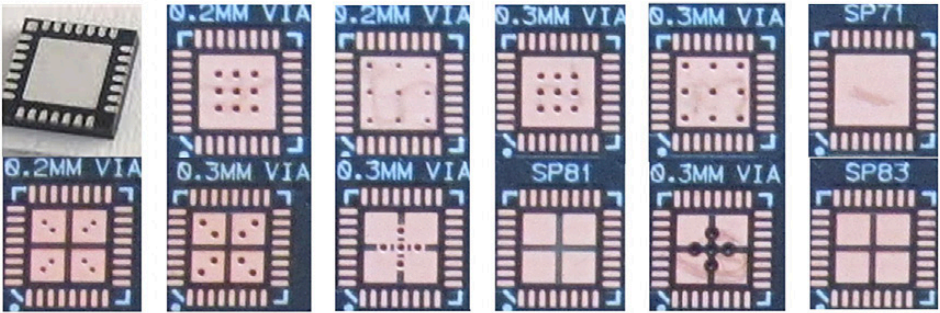


Figure 1.5: Examples of different board mask designs.

Component Placement

The placement force and Z-height can also affect voiding performance. It is important to optimize these settings before mass production has begun. If the parts are placed into the paste with too much force, the component standoff will be minimized, making it more difficult for the flux volatiles to outgas.

Reflow Profile

There are many ways that the reflow profile can be adjusted to help minimize voiding; it depends on the type of voiding that you are experiencing, as well as the components and solder paste that are being used. BTC voiding operates on very different mechanisms than BGA voiding. A soak profile may be better than a linear profile, but this is reliant on the specific solder paste in your process. Some solder pastes prefer a hot peak temperature, while others perform better with a short, fast profile. This is an area in the process where you may tweak and solve the voiding problem for one component, but by doing so, you may negatively impact another component. In the end, the name of the game is optimization, which should be done for each assembly prior to mass production.

Vacuum reflow equipment has also helped to minimize voiding in solder joints and is becoming more popular with builds where voiding is critical.

Summary

As you can see, the challenge of voiding is extremely complex. In the perpetual void-minimization quest, it is important to consider all the variables that could be affecting the outcome, and to optimize the process and the materials to achieve acceptable results. Although the factors that generate voids are many, it is possible to minimize voiding by adopting the parameters and standard processes described in this chapter. Stencil design, solder paste board design, component placement, and the reflow process are the key areas of focus.



Graping

The growth of personal electronic devices continues to drive the need for ever-smaller active and passive electrical components. This miniaturization trend, together with the demands for RoHS-compliant Pb-free assembly, has created more challenges, including the graping effect.

As a solder paste deposit decreases in size, the relative surface area of exposed solder particles increases, and the amount of available flux to remove surface oxides decreases. Compounding this is the additional heat necessary to reflow most Pb-free solders, resulting in a formula conducive to producing the graping phenomenon. During the heating process, as the flux viscosity decreases and begins to spread downward and outward, the solder particles are exposed at the top of the solder paste deposit. If there is no flux in proximity, these solder particles may become oxidized when the solder paste enters the ramp or soak stage of reflow. These oxides will inhibit the full coalescence of the particles into a uniform solder joint when the solder is liquidus. The unreflowed particles often exhibit the appearance of a cluster of grapes, as can be seen in Figure 2.1.

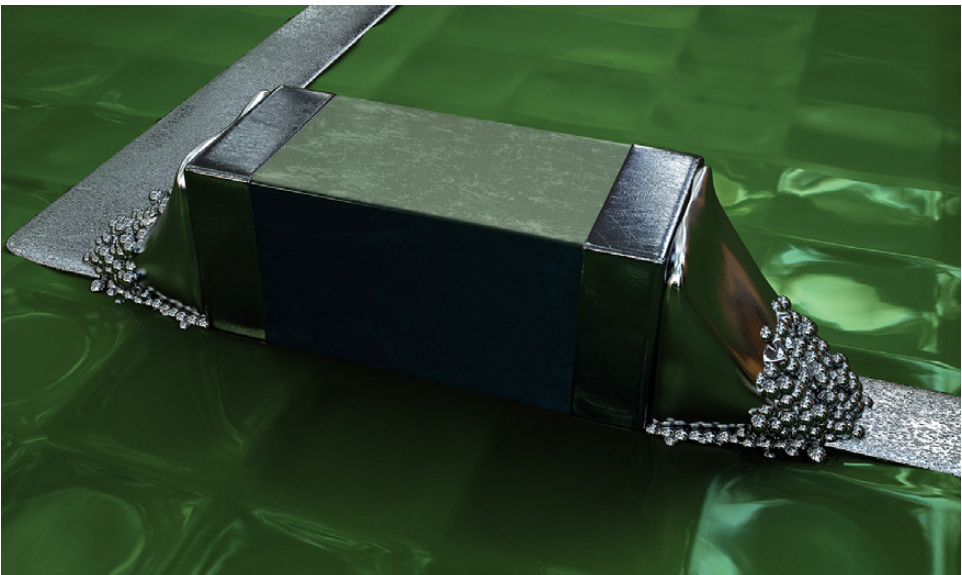


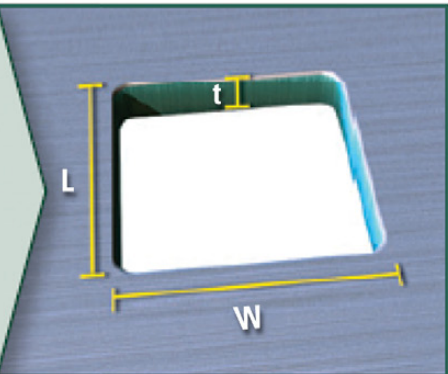
Figure 2.1: The graping effect.

Stencil Printing

The area ratio (AR) is a critical metric in successful stencil printing. It is defined as the area of the stencil aperture opening divided by the area of the aperture sidewalls. Figure 2.2 shows a schematic for square/rectangular and circular apertures. A simple calculation shows that the AR is simplified to the diameter (D) of the circle divided by four times the stencil thickness (t) or $AR=D/4t$. Somewhat surprisingly, the result is the same for square apertures, with D now equal to the sides of the square. For the AR of a rectangular aperture, the formula is a little more complicated: $ab/2(a+b)t$, where a and b are the sides of the rectangle.

Area Ratio For Square/Rectangular Apertures

$$\text{Area Ratio} = \frac{\text{Area Opening}}{\text{Area Walls}}$$
$$\text{Area Opening} = L \times W$$
$$\text{Area Walls} = 2t(L + W)$$
$$\text{Area Ratio} = \frac{L \times W}{2t(L + W)}$$



Area Ratio For Circular Apertures Sample Area Ratio Chart

$$\text{Area Ratio} = \frac{\text{Area Opening}}{\text{Area Walls}}$$
$$\text{Area Opening} = \frac{\pi D^2}{4}$$
$$\text{Area Walls} = \pi D t$$
$$\text{Area Ratio} = \frac{D}{4t}$$

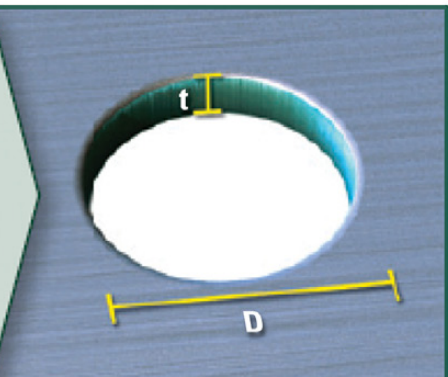


Figure 2.2: Aperture schematics for square/rectangular and circular apertures.

It is widely accepted in the industry that in order to get good stencil printing, the AR must be greater than 0.66. Experience has shown that if $AR < 0.66$, the transfer efficiency could be low and erratic, although this has gotten better with advances in solder paste technology.

Transfer Efficiency

Transfer efficiency, another important stencil printing metric, is defined as the volume of the solder paste deposit divided by the volume of the aperture. To accommodate fine-feature stencil printing, it is not uncommon to look at solder paste that incorporates finer powder in order to optimize the printing process. However, as the size of the powder particles within the solder paste decreases, the relative amount of surface area exposed increases. With this increase in surface area, an increase in total surface oxides is also introduced. This increase in surface oxides requires the flux chemicals to work even harder at removing the oxides and protecting the surfaces of the powder, component, and board metallizations during the entire reflow process.

On a 3 mil-thick stencil, the AR for a 6 mil square aperture is the same as the AR for a 6 mil circular aperture: 0.50. However, in comparing the two, the volume of the square solder paste deposit is greater (108 cubic mils) than the circular deposit (85 cubic mils). The additional solder paste volume provided by the square aperture may help reduce graping. Of greater importance, though, is the increased transfer efficiency provided by the square aperture. The square aperture design provides more consistent transfer efficiency, further reducing the potential for graping as inconsistent deposits could mean less volume.

SMD vs. NSMD Pads

Results from solder masking experiments have shown that the graping effect is less prevalent for the solder mask defined (SMD) pads. It is believed that the solder mask provides a barrier (dam), restricting the spread of the flux during the heating process, and increases the potential availability of the flux to remove oxides and protect from further oxidation. The solder mask can also act as a barrier to protect the solder paste powder particles in close proximity from further oxidation.

Water-Soluble vs. No-Clean

No-clean flux chemistries are generally rosin/resin-based (hereafter referred to only as resin) formulas. Because resins are not very soluble in the solvents used in water-soluble flux chemistries, they are typically replaced with large molecular compounds, such as polymers, in water-soluble fluxes. The

activator(s) within the flux chemistry removes the current oxides on the joining surfaces, as well as on the solder paste powder particles within the solder paste itself. Further oxidation/re-oxidation does occur during the heating stage. Whereas the resins in no-clean fluxes are excellent oxidation barriers and protect against re-oxidation, the lack of resins in water-soluble chemistries cause them to fall short in terms of providing oxidation resistance.

Hence, for the same reflow profiles—though water-soluble chemistries are generally more active—the lower oxidation resistance of water-soluble chemistries makes them more sensitive in long and/or hot profiles, increasing the potential for graping defects.

Ramp-to-Peak vs. Soak

For many years, the “soak type” reflow profile was quite prevalent. Over time, however, focus has shifted to ramp-to-peak (RTP) as the preferred reflow profile. Contributing to this shift are the higher reflow process temperatures associated with Pb-free solders, as well as the need to diminish the total heat exposure of the smaller paste deposits and temperature-sensitive components and board laminate. Another benefit of the soak profile is its utilization to reduce voiding. However, it is not as effective with Pb-free solders, due to the increased surface tension of Pb-free solders and the higher temperature used to reflow them. Figure 2.3 shows a soak and RTP (called linear in the figure) profiles.

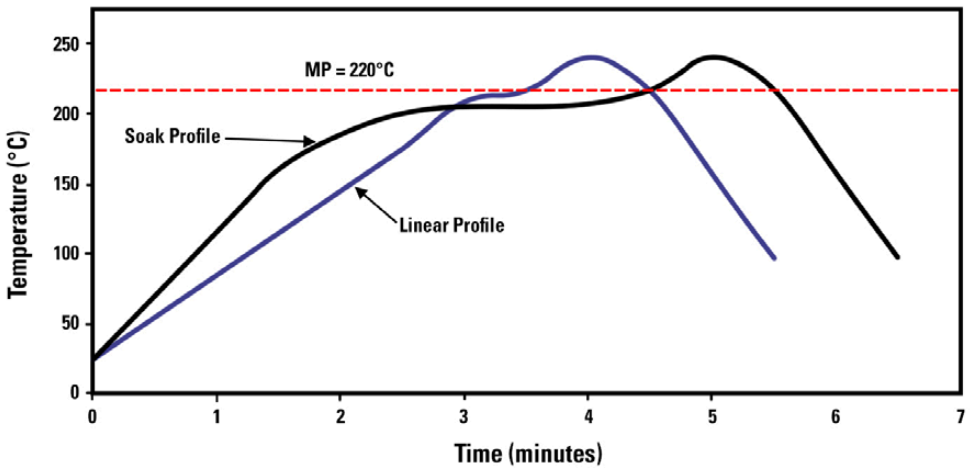


Figure 2.3: Typical reflow Pb-free profiles.

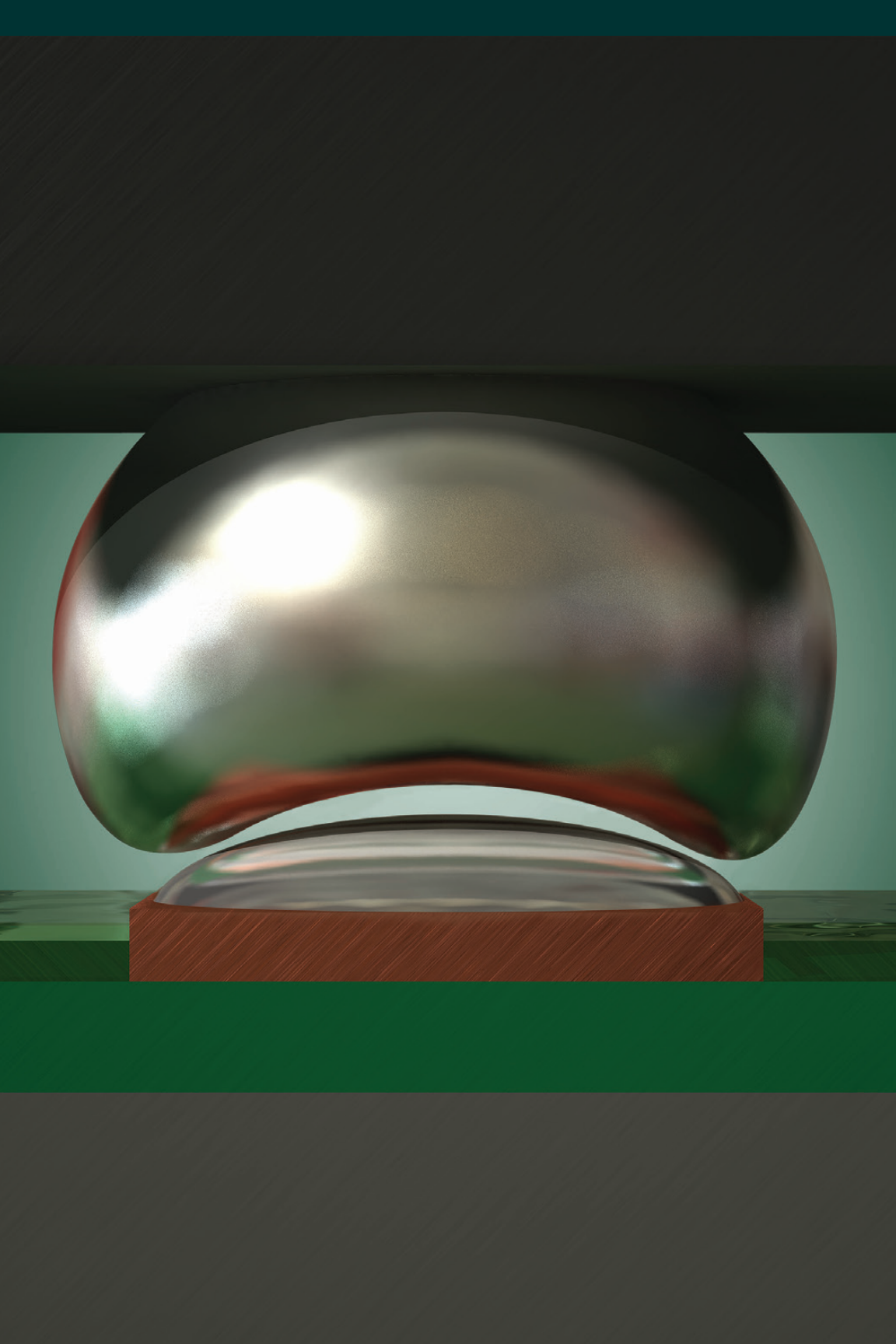
To minimize graping, a reduced oven time is better, provided you use the same time-above-liquidus (TAL) and peak temperature. The soak profile typically produces more graping than an RTP profile. The graping effect is exacerbated as the total time in the oven increases. Decreasing the total heat dramatically decreases the graping effect. A ramp rate (from ambient to peak) of 1°C/second is commonly recommended, which equates to approximately 3 minutes, 40 seconds to a peak temperature of 245°C.

Summary

To reduce the graping effect, it is vital to ensure an optimal printing and reflow process. Using the guidelines provided for the area ratio and good process/equipment setup will ensure good transfer efficiency. Though the area ratio for circular and square aperture designs may be equal, the potential for graping increases with circular aperture designs due to decreased paste volume and decreased transfer efficiency.

From a reflow standpoint, decreasing the total heat input will decrease the likelihood of the effect. Using an RTP-type profile with a ramp rate of ~1°C/second is suggested.

Material factors also influence the outcome. The observance of graping increases as the solder paste particle size decreases and the area of surface oxides increases. Water-soluble solder paste chemistries do not provide the oxidation barrier that resins do for no-clean chemistries and are more prone to the graping effect.



The Head-in-Pillow and Non-Wet Open Defects

The advent of the ball grid array (BGA) package about four decades ago laid the groundwork for the head-in-pillow (HIP) and non-wet open (NWO) defects to rear their heads during the more recent Pb-free solder era. The lower reflow soldering temperatures that SnPb solder required, as compared to Pb-free solder, were typically not enough to cause these defects. However, now that more than 75% of electronic assembly is Pb-free, the HIP and NWO defects are a major concern.

Causes of the HIP Defect

The HIP defect occurs when the solder paste and the BGA solder ball reflow, but do not coalesce. There are three types of HIP:

- ▶ Type 1: The BGA ball is so severely oxidized or contaminated that the solder paste flux cannot break through the oxide or contamination layer.
- ▶ Type 2: The BGA package warps during reflow, separating the BGA ball from the solder deposit. The ball and solder paste solders are solidified before the cooling of the BGA relieves the warping and brings the solder deposit and ball back together (Figure 3.1).
- ▶ Type 3: The solder ball is brought back into contact with the still-molten solder dome on the pad, but the oxide film on the ball prevents coalescence of the two solder bodies.

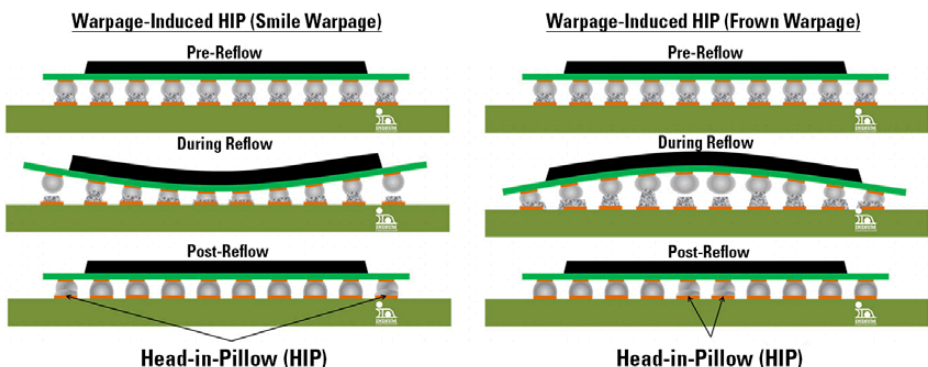


Figure 3.1: The steps in Type 2 HIP formation.

Causes of the NWO Defect

A non-wet open (NWO) is a defect that appears primarily on bumped components when assembled to a printed wiring board (PWB). The origin of the name for this defect is rather self-explanatory: an NWO is a lack of physical connection (an opening) between two surfaces that were meant to be soldered together. In many cases, opens occur between pads, leads, and terminations.

In this chapter, we will detail the lack of connection between bumped solder or BGA components and PWB pads. Non-wetting is the lack of a metallurgical bond that can be caused by a number of variables including, but not limited to: materials, reflow atmosphere, process, and PWB pad metallizations. We differentiate NWO defects from HIP defects, as they are mostly associated with pad metallizations, especially OSP.

In the case of an NWO defect, the solder paste, instead of staying on the pad, lifts off with the BGA solder ball when the BGA warps. The solder paste coalesces with the BGA ball during reflow, and when the BGA cools and warps back, a larger bump of solder is left with no trace of solder on the pad (Figure 3.2). Since the BGA solder ball may or may not be touching the pad, the open may not immediately be apparent, which could result in failures when the product is in the field.

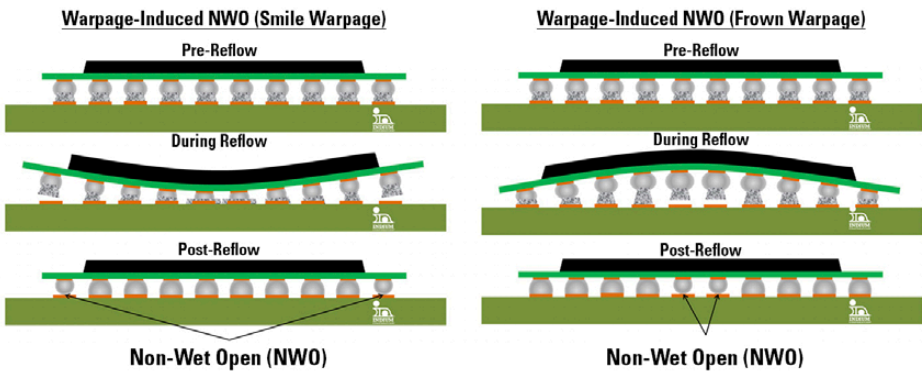


Figure 3.2: The steps in NWO formation.

NWOs occur most often at the perimeter of the BGA component, because when the component warps, the edges tend to pull up and away from the pads. When the surface tension of the solder paste is overcome, the solder is also pulled off the pads, causing it to coalesce with the solder bump. This component warpage is exacerbated by the drive toward thinner component substrates. Some BGA components end up looking like a potato chip when they go through the reflow process. This situation results in the solder paste having

to work harder to stay connected to both the pad and solder bump during the reflow process. Fortunately, some modern solder pastes are designed to facilitate this process.

Risk Posed by HIP and NWO

As shown in the rightmost image in Figure 3.1, the solder ball and solder paste dome are still in contact. Such a BGA might pass in-circuit testing (ICT), but fail in the field. Hence, HIP and NWO can be a considerable concern for field failures.

Detecting HIP/NWO Solder Joints

As discussed above, ICT will often miss HIP/NWO solder joints. In the past, dye and pry destructive tests were used. Two-dimensional X-ray techniques would often miss the defects, but modern three-dimensional X-ray systems can detect HIP/NWO solder joints effectively.

Overcoming the HIP/NWO Defects

PCB assemblers should work with their BGA component suppliers to ensure that BGA balls are not oxidized or contaminated. In addition to these concerns, another potential issue with high-Ag SAC alloys is “silver segregation,” which is caused by increased silver content on the surface of a BGA SAC solder ball. This concentration of silver and silver oxides obstructs the formation of a solder joint. This is a problem that must be resolved by the BGA manufacturer.

Oxidation, contamination, and silver segregation can result in Type 1 HIP. Since it is not warpage-dependent, it will typically be distributed randomly within the BGA balls.

Types 2 and 3 HIP will be exacerbated by poor solder paste printing. PCB assemblers should strictly avoid any application that prevents the solder paste from being printed squarely on the PWB pad with good transfer efficiency. This requires good stencil registration, proper PWB setup, and good stencil printer board support. Additionally, the stencil design should ensure that the area ratio of the BGA apertures is greater than 0.66. Laser-cut stainless steel or EFAB stencils will likely give the best results, but recent research suggests that nanocoating the stencils will produce better transfer efficiencies.

After stencil printing, solder paste deposits should be optically inspected to determine if they have printed squarely, with high transfer efficiency, and with low variation in volume from deposit to deposit. Figure 3.3 shows an undesirable situation that will likely produce HIP defects.

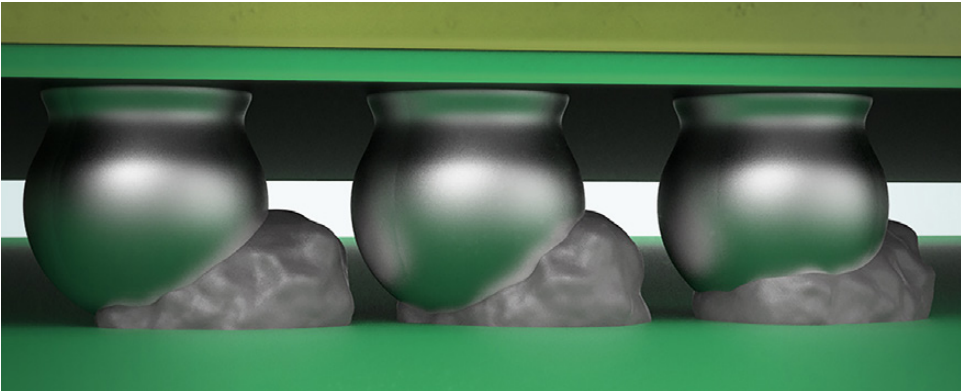


Figure 3.3: Poor registration of the BGA ball to the solder paste deposit will likely result in more HIP defects.

Solder paste can have a dramatic effect on avoiding HIP defects. HIP-resistant solder pastes should have excellent transfer efficiency, high tack, and a high oxygen barrier. Solder pastes with poor slump resistance are more prone to HIP defects because the gap between the paste and the ball increases when the component warps and the paste slumps. Solder pastes that have been developed to eliminate HIP defects tend to be more “elastic” so that they can bridge the gap between the board and the warping component. They also provide a strong oxidation barrier to protect the metallizations from further oxidation in the reflow process, good fluxing activity for fast wetting, excellent transfer efficiency with low variation between deposits, and enhanced slump resistance. These qualities allow the solder paste to adhere to—and stay with—the BGA ball if the BGA warps with increased temperatures in the reflow process.

Solder paste can be used to eliminate the HIP challenge altogether, and therefore, it is extremely important to make sure the solder paste you are using has outstanding HIP elimination properties. In one process, an assembler was experiencing 7% HIP defects. By switching to a solder paste developed to minimize HIP, the defect rate was reduced to 0% without making any other changes to the process.

In some cases, assemblers dip the BGA balls into a package-on-package (PoP) paste or PoP flux to increase the “height” of the ball and/or to ensure more flux activity/tack and oxidation protectant. Although this extra step has yielded some good results, this incorporates additional time and cost to the PCB assembly process.

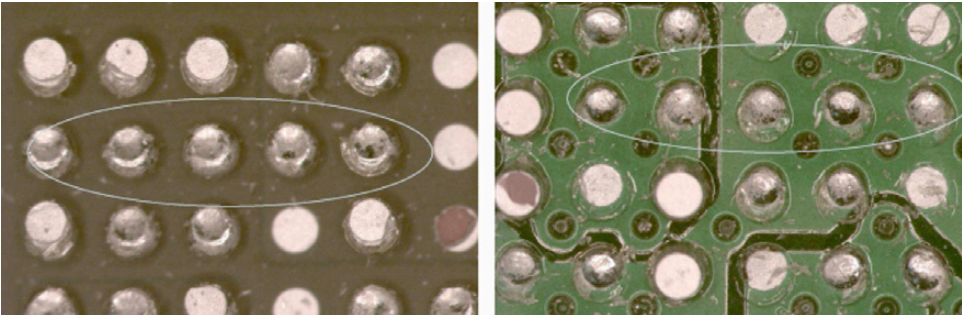


Figure 3.4: The mating surfaces of the BGA on the left and the PWB on the right in Type 2 HIP failures.

Types 2 and 3 HIP defects will typically be clustered together in rows due to the warping geometry (Figure 3.4).

The reflow profile can affect the formation of HIP defects. Typically, a slow ramp rate will minimize warping and slump. A common practice to minimize BGA voiding is a long soak profile, but this increases the oxidation rate of the metallizations, thus making HIP more likely. A hot and long time-above-liquidus (TAL) can aggravate warping and oxidation, and can also result in more HIP defects. It is important to minimize the heat input and TAL to reduce the risk of HIP defects. Once again, optimization is important to perform before mass production begins.

HIP-/NWO-Resistant Solder Pastes

Solder paste research scientists have developed pastes that resist HIP/NWO defects. These solder pastes have a strong oxidation barrier, good fluxing activity, and excellent slump resistance. They also provide excellent transfer efficiency in stencil printing and stick tenaciously to the BGA solder ball.

It is important to point out, though, that in some cases the inherent dynamic warpage of some BGA packages can be so extreme that the only solution is to work with the package supplier to minimize the package warpage.

Summary

Head-in-pillow and non-wet-open defects can be considerable challenges in the assembly of PCBs that have BGA component packages. By assuring that the BGA balls are not overoxidized or contaminated, that the solder paste deposit is squarely on the PWB pads with a good transfer efficiency, and that the reflow profile is not too rapid or hot, HIP defects can be minimized. In addition, solder pastes have been developed to minimize HIP defects even in processes that are not optimized.



PASSIVE
COMPONENTS

Tombstoning of Passive Components

Printed circuit board (PCB) issues can be a challenge, but not all of them can send your PCB to an early grave like tombstoning. Tombstoning is caused by unequal surface tension forces created during the melting of solder paste on opposite sides of a passive component. These unequal forces cause the passive component to lift up on one end and break contact with the circuit, resulting in something that looks eerily similar to a tombstone in a graveyard (Figure 4.1).

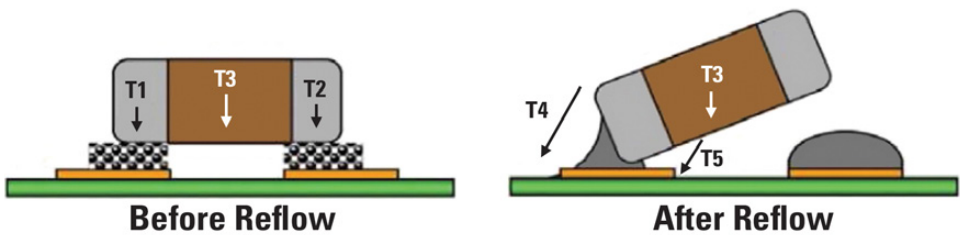


Figure 4.1: Tombstoned capacitor components.

Tombstoning Mechanism

Various factors contribute to tombstoning. Tombstoning is almost always the result of uneven wetting forces on the terminations of the component. When one end “wets” before the other, the now unbalanced wetting force of the solder “pulls” the component and rotates it, causing it to stand on end. We also encounter tombstoning following uneven heating of the PCB assembly. As the printed wiring board (PWB) travels through the reflow oven, the leading side of the passive component is often heated first (left side of passive in Figure 4.2). This uneven heating causes the solder paste deposit closest to the heat source

(the left side of Figure 4.2) to melt first. As this solder melts, its surface tension causes the passive to stand upright as seen in Figures 4.1 and 4.2.



T1 & T2: Tack Force

T3: Weight

T4: Surface Tension (outside)

T5: Surface Tension (underneath)

T4 is significantly higher using SnPb solder paste

Figure 4.2: The tombstoning mechanism in detail.

Solder Alloy

Another approach is to use a solder alloy that has a large “pasty” or “plastic” range as it melts. The plastic range is the range of temperature over which the solder is molten and solid. For a eutectic solder, such as Sn63/Pb37 solder, there is no plastic range, as the solder is completely solid at just under 183°C and completely liquid at just above 183°C. SnPbAg alloys, such as Sn62 or Indalloy®100, have been widely used to eliminate tombstoning issues with leaded assemblies due to their increased plastic range.

In Pb-free solders, SAC3510 (Sn/3.5Ag/1Cu) has a narrow plastic range, whereas SAC305 has a broader range. Therefore, one would expect SAC305 to perform better in terms of minimizing tombstoning—and it does. Figure 4.3 shows the results of experiments to determine the rate of tombstoning. Note that the tombstoning rate of SAC3510 is more than six times that of SAC305. Since SAC305 is one of the most common Pb-free alloys, the occurrence of tombstoning has greatly diminished in the Pb-free era.

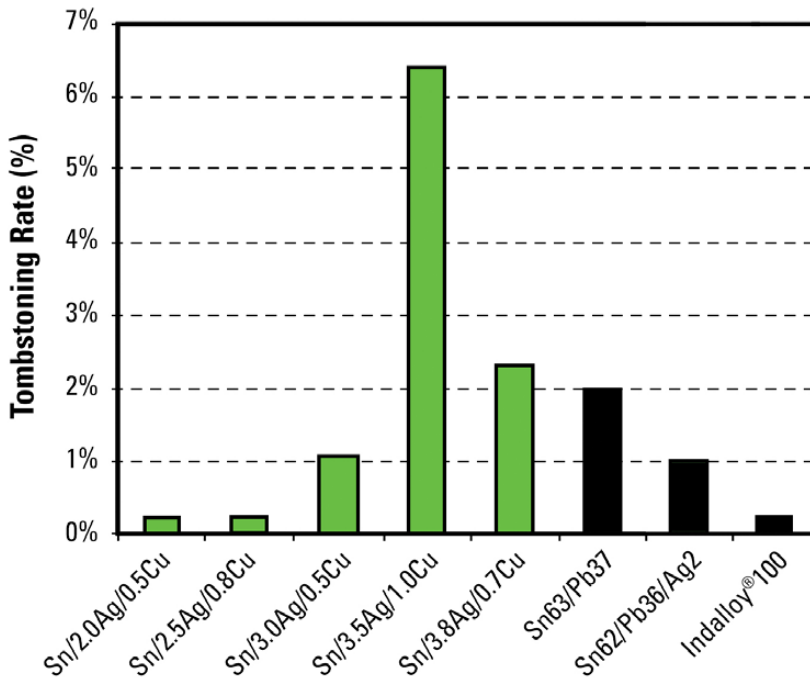


Figure 4.3: Alloy comparison of tombstoning other than SAC305. The green bars are lead-free alloys; the black are lead-containing alloys.

Board Design

It is extremely important for manufacturing engineers to work closely with design engineers to eliminate challenges and defects in PCB manufacturing. Tombstoning is one defect where proper design could eliminate the issue. If the board design has a heat-sink (a copper layer, for example) under or near one side of a passive component, and the other side is further away, the heat-sink could affect the thermal equilibrium of the assembly; the solder paste on the side without the heat-sink could go liquidus first, which could cause a tombstoning defect.

Stencil Design

Minimizing the amount of solder paste printed on the PCB pads will also reduce tombstoning. It is especially helpful to reduce the amount of solder printed directly behind the ends of the passive, which will eliminate nearly all

tombstoning forces. A typical stencil design to help achieve this goal is shown in Figure 4.4. In some experiments, this design completely eliminated tombstoning.

0402 Stencil Aperture Openings

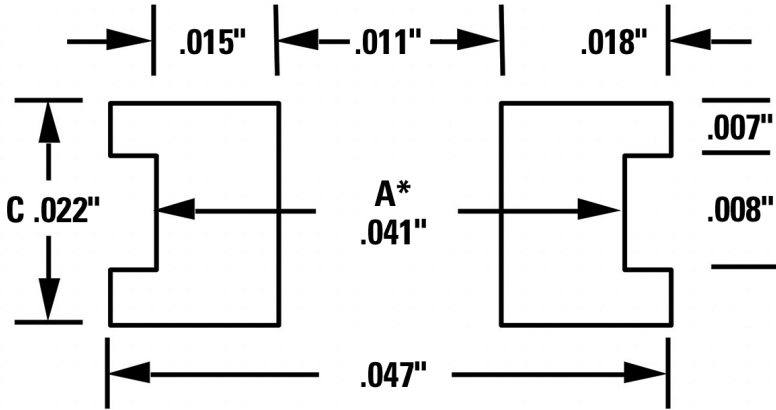


Figure 4.4: A stencil design to minimize tombstoning in 0402 passives.

Printing

The printing process and transfer efficiency are key components of many end-of-the-line defects, including tombstoning. If one side of a passive component has more solder paste present than the other side, the component may be placed in a position where it is contacting only the higher deposit. This would most likely result in a tombstone defect. The use of solder paste inspection (SPI) equipment can help ensure that solder paste deposits are within specification, and that one deposit is not higher than another. Optimization of the aperture's size and shape will also help minimize the variation of solder paste volume between pads.

Placement

Placement force and/or improper Z-height can often be the reason why tombstoning occurs. It is important to ensure that placement pressure and Z-height are appropriate for the assembly and optimized prior to production. It is also possible that the parts were placed with a skew. Although solder tends to self-align parts, if the component is placed wildly incorrectly, you could run into challenges.

Reflow

One approach to minimizing tombstoning is to decrease the total heat input during reflow by gradually increasing the ramp rate; however, this condition might be difficult to achieve in the reflow oven. Another option is to use a soak-type reflow profile to achieve thermal equilibrium between the two solder paste deposits so that both deposits enter the liquidus phase at the same time.

In addition to avoiding solders without a plastic range, a nitrogen atmosphere in the reflow oven tends to exacerbate tombstoning because nitrogen increases the wetting speeds and enables the surface tension forces to appear more rapidly. Unless there are fine-feature solder paste deposits or Package-on-Package (PoP) assemblies on the board, there most likely won't be a reason to use nitrogen, as most top-tier modern solder pastes can perform well in an air reflow atmosphere.

Summary

Tombstoning can be minimized by following the guidelines laid out in this chapter. A reliable way to minimize tombstoning is to use a solder alloy that has a large plastic range, such as Indalloy[®]100 (lead) or SAC305 (Pb-free). It is also important to keep an open dialogue with the board designers to minimize heat-sinks near or under one side of the passive components. Use a reflow soldering temperature profile that slowly moves through the solidus to liquidus, or minimizes thermal mismatch with a soak. Incorporate SPI to ensure that the solder deposits are similar heights and within specification, and print a solder deposit that is small, especially at the two ends of the passive. Ensure the placement pressure and Z-height are appropriate and the parts are not placed with a skew. Avoid using nitrogen in the reflow oven; with a good solder paste, it is unnecessary and exacerbates tombstoning.



Solder Paste Insufficients

Although a source for this statistic cannot be found, it is widely believed by industry experts that approximately two-thirds of the end-of-the-line defects in electronics assembly can be traced back to the stencil printing process. Therefore, a proper amount of solder paste printed squarely on the printed wiring board (PWB) pad is the best safeguard for good end-of-the-line yields. In this chapter, we will assume the solder paste is deposited squarely on the PWB pads and focus on how to ensure the amount of solder paste is adequate and consistent (Figure 5.1).

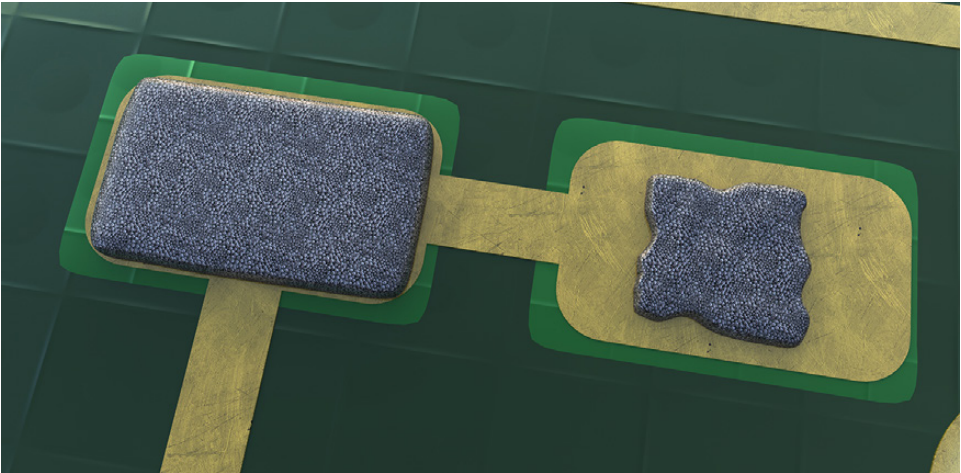


Figure 5.1: A good solder print vs. an insufficient solder print.

The Basics

To ensure successful stencil printing, a few basics are required. First, work with your solder paste supplier to ensure you are using a high-quality solder paste. This paste should have good response-to-pause and a long stencil life, and should not exhibit issues such as squeegee hang-up. Some assemblers may try to save pennies per gram up-front by purchasing a subpar solder paste, but end up ruining a several hundred-dollar PCB for a \$1,000 smartphone. This is compounded when talking about tens of thousands of dollars in boards, with applications like servers or super computers.

The stencil printer should be set up according to the solder paste and printer manufacturers' specifications. This might include: the correct squeegee (metal preferred) and squeegee speed; board support; and regular stencil wiping. Your solder paste and stencil printer providers work in the world of stencil printing every day and should be your first resource for advice on any of these topics.

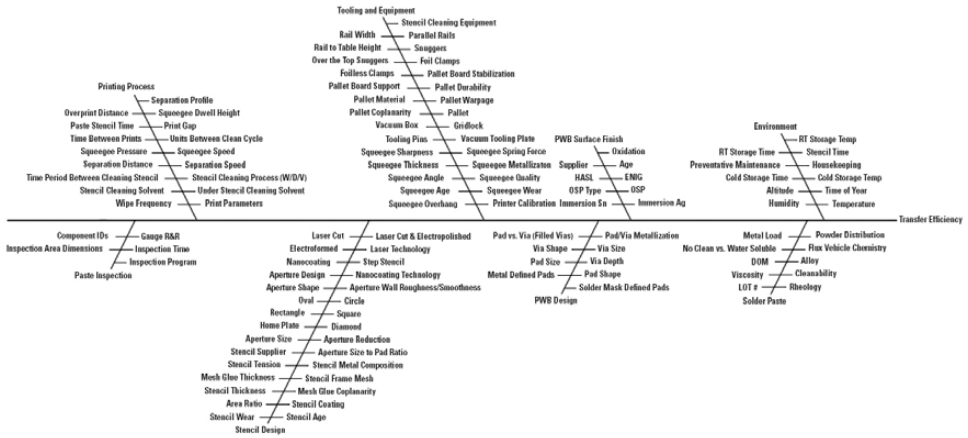


Figure 5.2: Ishikawa diagram of variables that play a role in transfer efficiency.

Besides solder paste performance attributes and composition, there are hundreds of other potential variables in the printing process that could cause solder paste insufficient defects. The Ishikawa diagram in Figure 5.2 helps to depict some of the more common causes within the manufacturing environment and process that could lead to solder paste insufficiencies. The natural first thought when solder insufficiencies occur is to focus on the solder paste performance, but this diagram is quite useful to refer to, as it will help broaden the search for the true root cause. Oftentimes, it is something other than the solder paste that is causing the defect. As you can see, the solder paste printing process is riddled with potential for insufficient solder paste deposits, due to the vast array of variables that play a role. It is extremely important to take the time to optimize the printing process prior to mass production.

Metrics Affecting the Volume of the Solder Paste Deposit

Transfer efficiency is the ratio between the volume of the stencil-printed deposit and the volume of the stencil aperture, expressed as a percent. In almost all cases, a transfer efficiency of 100% is ideal; however, most specifications will tell you that transfer efficiency between 50% and 150% is reasonable and achievable. For smaller fine-feature apertures found on 01005 or 0.3mm

pitch components, the transfer efficiency specifications are typically relaxed to between 40% and 140%.

To ensure that the transfer efficiency is high, the aspect ratio for a rectangular stencil aperture should be greater than 1.5. The aspect ratio is the width of the aperture (W) divided by the stencil thickness (t) as shown in Figure 5.3.

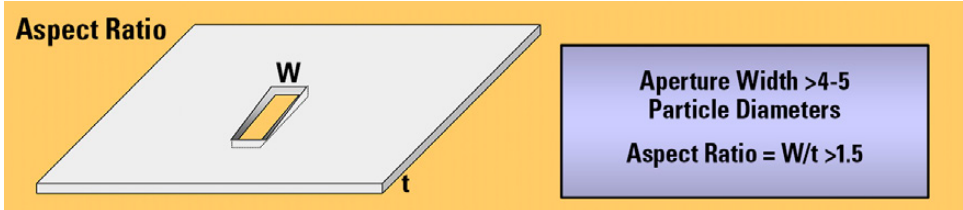


Figure 5.3: The aspect ratio for rectangular apertures should be greater than 1.5.

The area ratio is the area of the stencil opening divided by the area of the aperture sidewalls. For circular or square apertures, the area ratio should be greater than 0.66 (Figure 5.4). However, with miniaturization of components and the progression of solder pastes over the years, a minimum of 0.6 has become more acceptable and feasible. Whenever possible, it is better to use square apertures, as they provide more solder paste when the square side is equal to the circular diameter. Square apertures have also been shown to have better solder paste release, typically resulting in better transfer efficiency and lower variation between prints. Rounded corners can help to maximize square apertures' performance even further.

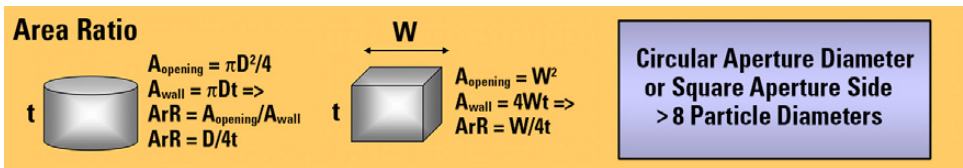


Figure 5.4: The area ratio for circular or square apertures should be >0.66.

Experience has shown that for successful printing, the rectangular aperture width should be greater than five times the largest solder powder diameter. For circular or square apertures, the diameter should be greater than eight times the largest solder powder diameter. The reason for the difference is that for a rectangular aperture, five balls will be "stacked" on five balls for the entire length of the aperture. For circular apertures, if five balls fill the diameter, the remainder of the circle can accommodate less than five balls due to its curvature. The powder size distribution of the particle diameters for Types 3, 4, 5, and 6 solder pastes is shown in Figure 5.5.

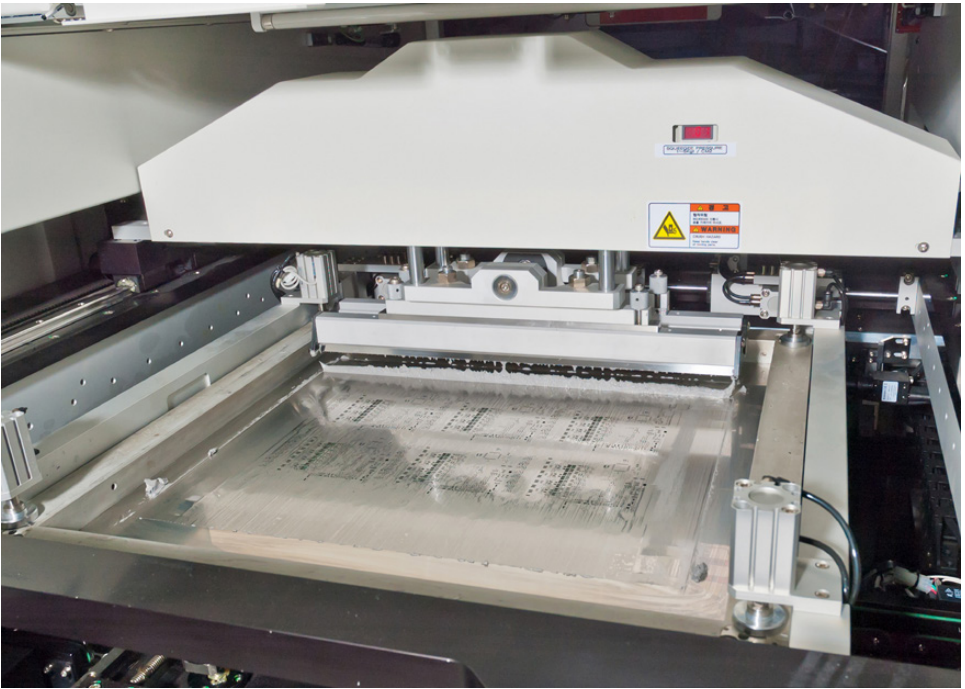
Powder Size (Type)	Diameter Range (microns)	
3	25	45
4	20	38
5	15	25
6	5	15

Figure 5.5: Solder powder diameter distributions vs. powder type.

Example Calculation

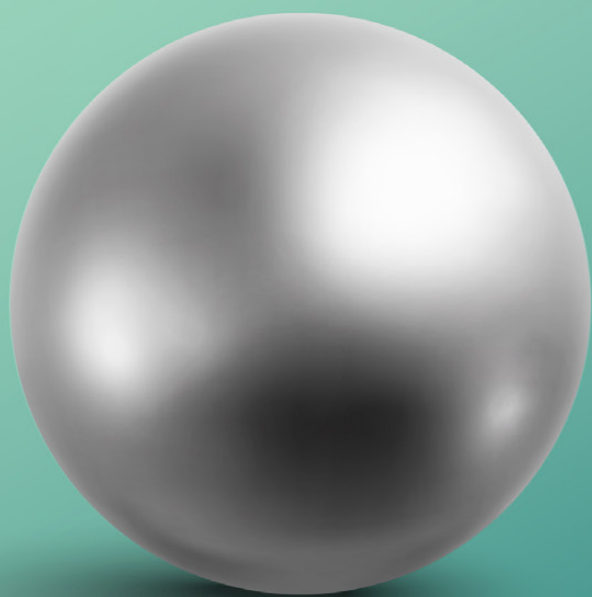
As an example, consider an application with a 4 mil (0.004" or 0.10 mm) thick stencil. The PWB has 0.4 mm spacing for rectangular apertures. The apertures are 0.2 mm in width. The aspect ratio is then $0.2/0.1 = 2$. So, the aspect ratio is good. A Type 4 solder paste is planned. The maximum powder size for a Type 4 solder paste (according to Figure 5.5) is 38 microns or 0.038 mm. 5×0.038 mm is 0.19 mm, so a Type 4 powder is appropriate. The PCB also has chip-scale packages with 30 mil (0.75 mm) spacing. The pad width is 12 mil (0.30 mm). The area ratio is $D/4t = 0.30 / (4 \times 0.1) = 0.75$. Since this is greater than 0.66, the area ratio is okay. Eight times the maximum ball diameter is $8 \times 0.038 = 0.304$; this is a bit above the 0.30 mm stencil aperture. This situation is probably acceptable because it is only off by 1% and these are rules of thumb, not laws. One reason to avoid finer solder powder types, unless it is required, is that their extreme surface area-to-volume ratio can exacerbate other defects, such as the graping effect.

Although performing these calculations can be tedious, there is a free software program that can make these calculations easy. StencilCoach® is a tool that can calculate aspect and area ratios, and determine the solder powder type needed. It can also perform other stencil-related calculations, such as aperture design to minimize solder balling and aperture design for the pin-in-paste process.



Summary

A proper amount of solder paste printed squarely on the PWB pad is the strongest factor for determining good end-of-the-line yields. After ensuring your solder paste has a long stencil life, good tack and reflow performance, and excels in response-to-pause, it is vital to ensure that the transfer efficiency is between 50% and 150%. This goal can be achieved by optimizing the printing process, ensuring that the aspect ratio for rectangular stencils is greater than 1.5, and following the five-ball rule. For circular or square apertures, the area ratio should be greater than 0.66 and the eight-ball rule should be followed.



Solder Balling and Beading

Solder paste creates the necessary bonds between component leads and printed wiring board (PWB) pads in the surface mount technology (SMT) assembly process. When formed correctly, these solder joints provide a high-yield and high-quality printed circuit board (PCB) assembly. Formed incorrectly, these joints can cause defects, which lead to field failures and reduce the reliability of the end-product.

One of the most commonly observed defects in the SMT assembly process is solder balling. Solder balling occurs when small solder particles, which did not coalesce with the main solder pool in the reflow process, are scattered near the solder joint. When the balls are large, they are typically referred to as solder beads (Figure 6.1). Solder beading is especially common around very low-standoff components or passive components, such as chip capacitors and resistors. For simplicity, we will just refer to solder balls in this chapter, no matter the size.

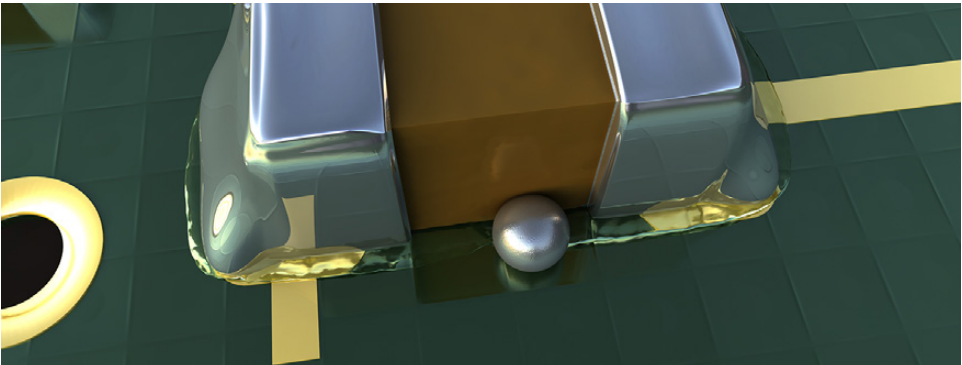


Figure 6.1: A solder ball formed after reflow on a passive discrete component.

Solder balls may cause electrical shorts (either immediately or in the future) if the balls are dislodged and move around on the PCB. Shorts are especially likely when solder particles are located between components or leads in fine-pitch components. Since solder balls are formed from solder paste particles that have not coalesced with the main solder joints, their formation could lead to insufficient solder in the joints. The current drive for smaller components

and finer PWB pitches, as well as the demand for no-clean assembly processes, makes it essential that SMT assembly processes are solder ball-free.

Since solder balls are quite common, it is important to be familiar with the different ways in which they can occur. Examining where they form in relation to the pad area is essential in determining their cause. When solder balls are formed away from the pad area, it is most likely due to moisture absorption by the solder paste. Such moisture absorption can occur if a refrigerated paste was opened before reaching room temperature. If the solder balls and beads form around the PWB pad area, they are more likely from solder pastes with fine solder powders or the result of overheated flux during reflow.

The Primary Cause in Passive Components: Stencil Aperture Design

The primary cause of solder ball formation in passive components is stencil design. If the stencil apertures are the shape of the PWB pad, an excess of solder paste can occur in the innermost part of each pad. This excess of solder can then result in solder balls forming during the reflow process, as shown in Figure 6.1. A stencil design that has been shown to virtually eliminate solder balls is the "home plate" design (Figure 6.2). The reason for the success of the home plate design is the reduction of solder paste in the innermost part of the PWB pads. Others have shown that simply reducing the "D" dimension in Figure 6.2 and keeping the rectangular aperture shape is also effective.

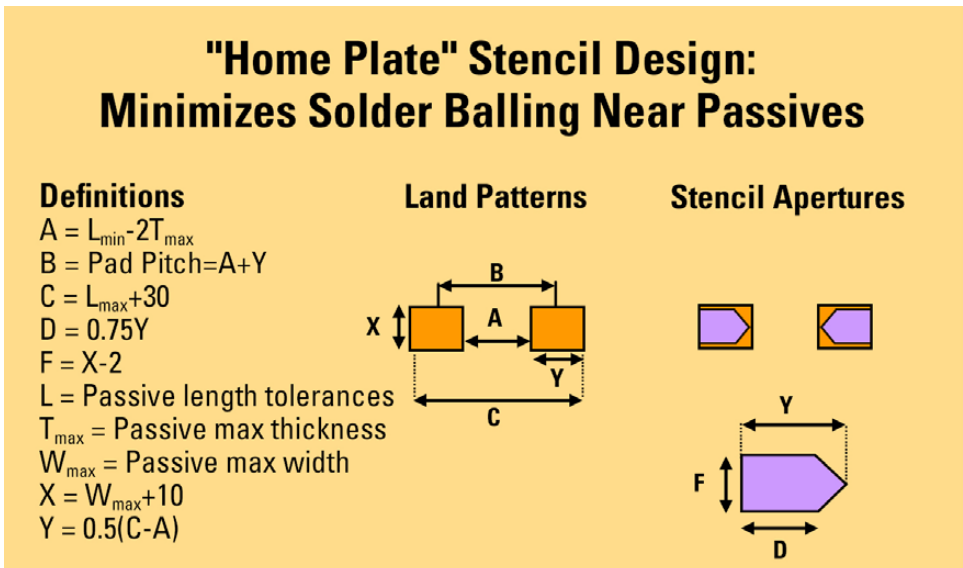


Figure 6.2: The "home plate" aperture design virtually eliminates solder balling in passive components.

In the following sections, we will discuss other approaches to reduce solder balling for other types of components.

Process-Induced Causes During Printing and Placement

Stencil: Poor gasketing can cause a buildup of solder paste under the stencil, which can later be transferred to the PWB in unwanted areas and result in solder balls. Poor gasketing can be the result of poor stencil alignment, PWB shrink, the stencil aperture being larger than the PWB pad, the pad being smaller than the aperture, solder paste on the bottom of the stencil, solder mask on the pad, or a hot air solder level (HASL) dome. All of these gasketing issues are shown in Figure 6.3.

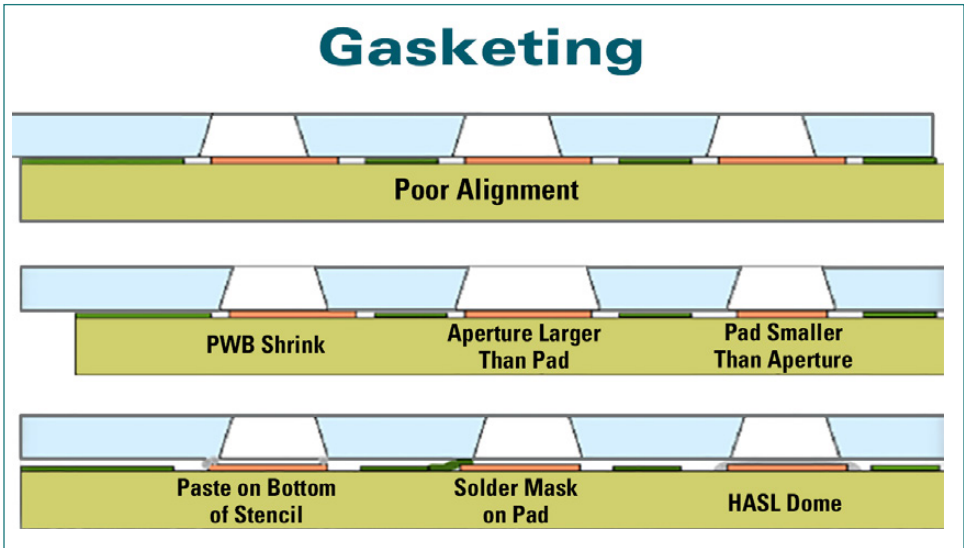


Figure 6.3: The causes of poor gasketing (Source: *The Art of Stencil Printing*, Steve Arneson, ASC International, SMTA Workshop April 7, 2015).

Board design: PWB pad design or substrate metallization can contribute to increased rates of solder balling. Sometimes, during the manufacture of the PWB, the solder mask between adjacent pads is skipped, causing solder balling during the assembly process because there is no solder repellant on the metallization. The pad locations, if placed too close together, can also result in increased solder balling.

Solder mask: The solder mask may release volatiles during reflow that can interact with the paste and cause solder balling. These volatiles can cause the solder paste to splatter, resulting in solder balls within the area of the PWB pad.

Poor solderability of component leads or substrate metallization:

Excessive oxidation of the leads or substrate metallization will increase the probability of solder balling, as most of the flux is used to remove the oxides. This situation leaves less flux during the actual reflow process, to counteract the new oxides that are formed. This situation may result in the solder poorly wetting the pad, thus increasing the chance of solder balling. Using a nitrogen reflow atmosphere can help prevent this condition, because nitrogen will inhibit or slow down the rate at which new oxides are formed.

Print or placement pressure: Excessive pressure during stencil printing can cause the solder paste to bleed out. Bleed-out is also common when the component placement pressure is too high, forcing the solder paste to squeeze out from the pads. The excessive solder paste caused by bleed-out can then cause solder balls during reflow.

Misalignment during printing and/or placement: Misalignment of the solder paste deposit can be caused by incorrect registration of the boards during solder paste printing, whereas misalignment of the component can occur during component placement. Both of these situations can result in excess solder on either side of the pad. During reflow, this excess solder may form a solder ball.

Cleaning: Inefficient wipe methods can cause solder paste residue remaining on a stencil to be accidentally smeared or deposited onto the next board. This unwanted solder paste can form a solder ball during the reflow process.

Process-Induced Causes During Reflow

Ramp-up/preheat rate: A fast preheat rate will not allow the volatile solvents to vaporize, which may lead to spattering during reflow. Research conducted by Lea³ shows that increasing the preheat time would reduce solder balling. However, overdrying the solder paste may lead to increased oxidation of the powder, thereby leading to another cause of solder balling. Additionally, a fast ramp rate can cause spattering. To prevent that, a slower ramp rate, typically <1.5°C/second from room temperature, is recommended.

Soak time: Adding or increasing soak time will help equalize the substrate and component temperatures to allow for equal wetting of the solder. Increasing time above liquidus will help to allow for the complete flow of the liquid solder before it begins to cool down. These approaches will minimize solder ball formation.

Reflow atmosphere: Nitrogen reflow can significantly reduce solder balling for solder pastes with insufficient fluxing capacity, as the hot air during air reflow can increase oxidation of the solder paste, which leads to solder balling.

Solder Paste Concerns

Handling of paste: Used and fresh solder paste should not be mixed together. Used solder paste can contain water that has been absorbed from the atmosphere, which can cause spattering during reflow. Additionally, opening refrigerated solder paste before it reaches room temperature can also lead to moisture absorption by the solder paste. Solder paste should not be returned to the refrigerator; if the solder paste has already absorbed moisture, it will cause condensation on the lid when the paste is cooled.

Exposure to humidity: Humidity will increase the oxidation of the powder and increase the moisture content of the solder paste, both of which can lead to increased rates of solder balling. Humidity increases oxidation by enabling the oxygen to be more reactive, but the spattering caused by humidity is likely the greater cause of solder balling. Solder pastes react to humidity differently based on the nature of the flux vehicle (the chemicals employed). Water-soluble solder pastes are hygroscopic, so they tend to have a shorter stencil life. With the advances in flux technology over the years, new solder paste formulations have higher humidity tolerances.

Solder paste slump: Excessive solder paste slump (cold and hot) can increase solder balling and beading. Slump-resistant solder pastes have been developed, so these types of solder pastes should be used, if possible.

Wicking effect: Wicking is a redistribution of solder away from the intended joint from one deposit to another caused by the solder's surface tension. If there is a tight tolerance between components or pads, the solder mask may draw the solder paste away from the component, leading to solder balling.

Insufficient flux capacity: If the flux activity is too low, or if there are too many oxides or contaminants present, the flux may not sufficiently clean the oxides. When the oxides are not properly cleaned, the solder powder may not wet together and form one solder joint, but may split into solder balls.

Particle size: The number of solder balls increase as the particle size decreases. Since there are more powder particles present, the probability of having some particles left out during coalescence increases. Smaller particle sizes also have

more oxides present, since more surface area is exposed. Finer particle sizes can also tend to slump more readily.

Flux and moisture outgassing: Solder balls are mainly caused by the outgassing of flux at rates higher than the cohesive force of the solder paste, usually during the preheat stage of the reflow process. During the outgassing of the flux, isolated solder paste is formed. These newly formed aggregates will melt and coalesce separately; when these aggregates occur away from the component, they form solder balls. Excessive moisture in the solder paste can also cause spattering, which may emerge as solder balls.

Flux activation temperature: The rate of solder balling decreases as the flux activation temperature decreases. This effect occurs because a lower activation temperature will encourage powder particles to cold weld during preheating.

Metal load: Higher metal loads decrease solder balling rates, as the densely packed powders have an increased probability of cold welding together. A higher metal load means that the solder paste is more viscous, so there is less flux available to be outgassed, and the flux vehicle is better able to retain its integrity and avoid slumping.

Excessive solder powder oxides or contaminants: The more oxides present, the more barriers solder powder particles will need to overcome in order to coalesce together. This situation also drives up the activation temperature, which invariably increases solder ball formation.

Summary

After examining the various causes of solder balling and beading, it's important to identify how to adjust a process or product formulation to achieve a solder ball-free PCB. In summary, here are some recommended changes:

- ▶ For passive components, the number one solution to solder balling is a reduced stencil size design like the "home plate" design.
- ▶ Ensure the components and substrates have excellent solderability.
- ▶ Avoid using too much pressure during printing and placement.
- ▶ Check the stencil to ensure good gasketing and a clean wipe.

- ▶ Control the environmental humidity (relative humidity of no more than 50% is preferred).
- ▶ Practice good solder paste handling techniques; consult your solder paste manufacturer for recommendations.
- ▶ Avoid scavenging leftover solder paste; this includes returning used solder paste to the refrigerator or mixing it with fresh paste.
- ▶ Do not leave solder paste on the stencil for future use, especially hygroscopic pastes.
- ▶ Select the proper solder mask material and thickness to avoid interaction with the solder paste.
- ▶ Optimize the reflow profile and method selected (not too long or short). Reduce preheat temperature and ramp rate. Ask your paste vendor for the recommended solder paste reflow profile.
- ▶ Reduce the amount of solder paste printed by reducing the aperture size or stencil thickness. Aperture design modification is a common approach for reducing solder beads or balling.
- ▶ Adjust your board design to increase the spacing between adjacent pads to prevent solder balling.
- ▶ Ensure proper registration during printing and component placement.
- ▶ Prebake components or boards to remove moisture and volatiles that could interact with the solder paste.
- ▶ Ensure the solder paste has sufficient flux activity and capacity.
- ▶ Adjust the flux formulation to reduce slump, hygroscopic tendencies, and the activation temperature.
- ▶ Using fine particles increases the number of particles that can be carried away during heating; use coarse powder as much as you can.
- ▶ Reduce the presence of oxides and contaminants in the powder.
- ▶ Increase the metal load of the paste.
- ▶ Adjust flux volatiles to reduce spattering during reflow.
- ▶ Consult your solder paste supplier to optimize these material changes.

Conclusion

Our world today is more dependent than ever on electronics. Yet, the arrival of lead-free solders in 2006 and the constant miniaturization of components have made assembling the circuit boards in electronic products more challenging than ever.

To minimize the risk of defects, it is best to start with the process recommendations in the solder paste specifications and the process rules of thumb for stencil design and reflow parameters mentioned in this book.

If certain potential defects are a concern, such as BTC voids, follow the recommendations in this book.

It is important to remember that preventing potential defects is an optimization process. As such, minimizing one defect may affect another. As an example, the type of reflow profile to minimize BTC voiding (Figure 1.1) may exacerbate graping. Minimizing graping is best served by a ramp-to-peak reflow profile such as in Figure 2.3.

Finally, it cannot be overstressed how helpful your materials and equipment providers can be. The folks in these companies deal with defects and electronic circuit board challenges every day. They literally have “seen it all.” Therefore, we recommend contacting them early on if you have defect issues or are uncertain how to set up a process to assemble a new or different PWB.

References

1. J. A. DeVore, 1984, "To Solder Easily: The Mechanisms of Solderability and Solderability-Related Failures," *Circuits Manufacturing*, pp. 62-70.
2. Indium Corporation, "[Reducing Solder Beads and Solder Balls](#)," Application Note.
3. C. Lea, 1988, *A Scientific Guide to Surface Mount Technology*, Electrochemical Publications, United Kingdom: Isle of Man.
4. N.C. Lee, 2002, *Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP and Flip-Chip Technologies*, Boston (MA): Newnes Publications, pp. 133-141.
5. P. Zarrow and J. Hall, 2019, *Electronics Assembly Boot Camp*, Springfield (TN): ITM Consulting USA, p. 79.





About Indium Corporation

Indium Corporation is a premier materials refiner, smelter, manufacturer, and supplier to the global electronics, semiconductor, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and Nano-Foil®. Founded in 1934, the company has global technical support and factories

Located in China, Germany, India, Malaysia, Singapore, South Korea, the United Kingdom, and the USA.

Indium Corporation's InSIDER Series is a free program designed to deliver expert technical content, share industry knowledge, and promote professional growth using a virtual platform. Current and future webinars can be found at: indium.com/webinar.

Defects Eliminated, Reliability Delivered

AVOID: DENDRITIC GROWTH

AVOID: VOIDING

AVOID: SOLDER BEADING

AVOID: HEAD-IN-PILLOW

AVOID: NON-WET OPENS

AVOID: INSUFFICIENT SOLDER DEPOSITS

AVOID: CRACKING

Indium8.9HF Solder Paste

Indium8.9HF Solder Paste

From One Engineer To Another®

For more information about
Indium8.9HF Solder Paste, visit:
www.indium.com/SD007

